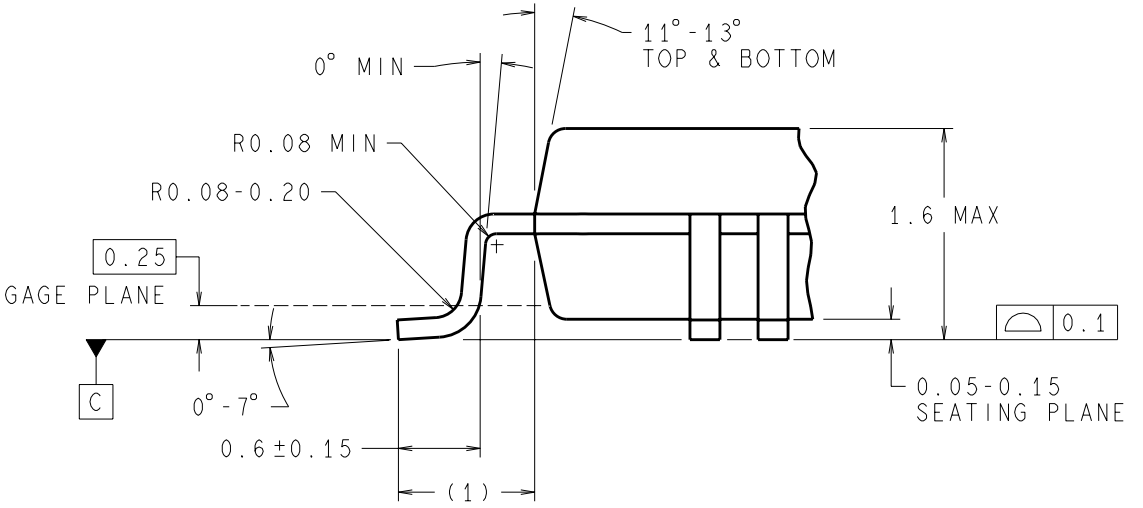
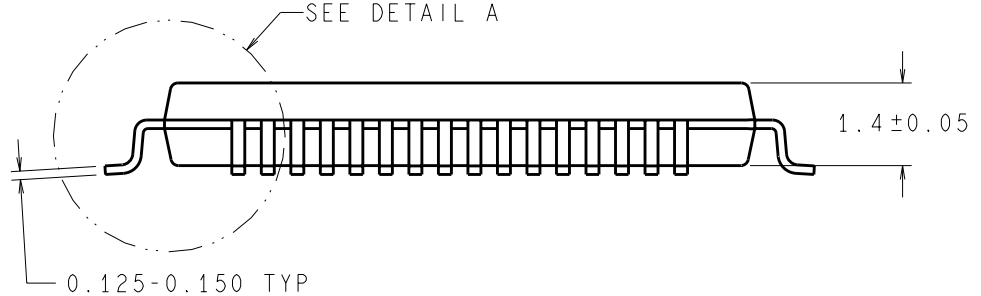
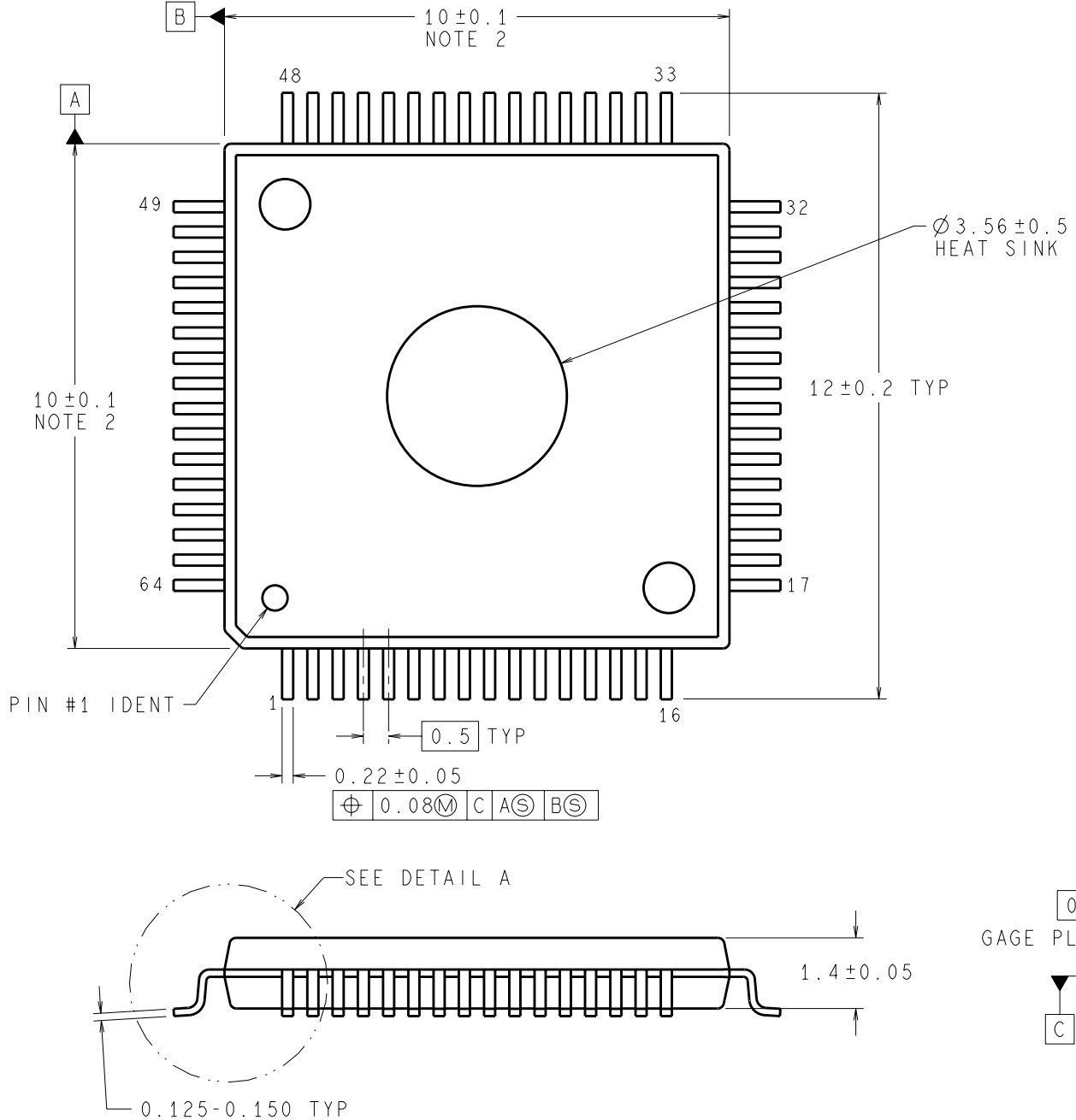


REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11589	10/07/1996	MS/SM
B	TITLE: LOFP WAS TOFP; UPDATE NOTE 3; ADD GEOMETRIC TOLERANCE	12317	11/10/1999	TL/RW



DIMENSIONS ARE IN MILLIMETERS

DETAIL A  
TYP, SCALE: 30X

NOTES: UNLESS OTHERWISE SPECIFIED

- STANDARD LEAD FINISH:  
7.62 MICROMETERS MINIMUM SOLDER PLATING (85/15)  
THICKNESS ON ALLOY 42/ COPPER.
- DIMENSION DOES NOT INCLUDE MOLD PROTRUSION.  
MAXIMUM ALLOWABLE MOLD PROTRUSION 0.25mm PER SIDE.
- REFERENCE JEDEC STANDARD MS-026, VARIATION BCD,  
DATED FEBRUARY 1999.

APPROVALS	DATE	National Semiconductor			
DRAWN <b>MARTA SUCHY</b>	10/07/1996	2900 Semiconductor Dr., Santa Clara, CA 95052-8090			
DFTG. CHK. <b>MARTA SUCHY</b>	11/10/1999	<b>LOFP, JEDEC METRIC, 10 X 10 X 1.4mm, 64 LEAD, EXPOSED H/S</b>			
ENGR. CHK. <b>RANDY WALBERG</b>	11/10/1999				
		SCALE <b>N/A</b>	SIZE <b>C</b>	DRAWING NUMBER <b>(SC)MKT-VEV64A</b>	REV <b>B</b>
		FORMERLY: N/A	SHEET 1 of 1		